63. (New) A microelectronic structure comprising:

a substrate;

a gate electrode formed over the substrate and defining an underlying channel region in the substrate;

a source/drain formed in the substrate adjacent the gate electrode and having an activated doped region with a first silicide layer disposed therein and wherein the activated doped region and the first silicide layer are aligned with a spacer disposed along sidewalls of the gate electrode; and

the source/drain also having an extension of the activated doped region wherein the extension has less dopant concentration than the activated doped region and the extension and a second silicide layer disposed in the extension are aligned with the gate electrode to have the less dopant concentration of the extension reside between the channel region and the activated doped region.

64. (New) The microelectronic structure of claim 63, wherein the activated doped region is thicker than the extension.

65. (New) The microelectronic structure of claim 63, wherein the first silicide layer is thicker than the second silicide layer.

66. (New) The microelectronic structure of claim 63, wherein the activated doped region and the extension comprise ion implanted material.

67. (New) The microelectronic structure of claim 63, wherein the first and second silicide layers comprise different metals.

68. (New) The microelectronic structure of claim 63, wherein the first and second silicide layers comprise a same metal.

69. (New) The microelectronic structure of claim 63, wherein the second silicide layer comprises $CoSi_2$.

70. (New) The microelectronic structure of claim 63, wherein the second silicide layer comprises $TiSi_2$.

71. (New) The microelectronic structure of claim 63, wherein the first silicide layer comprises nickel silicide.

72. (New) The microelectronic structure of claim 63, wherein the first silicide layer comprises $CoSi_2$.

73. (New) The microelectronic structure of claim 63, wherein the first silicide layer comprises $TiSi_2$.

Sub F3

74. (New) The microelectronic structure of claim 63, further comprising a barrier layer adjacent the gate electrode.

75. (New) The microelectronic structure of claim 74, wherein the barrier layer comprises silicon nitride.

E1

76. (New) The microelectronic structure of claim 63, wherein the extension is approximately 300-500 angstroms in thickness.

77. (New) A source, drain and gate structure comprising:

a semiconductor substrate;

a gate electrode formed over the substrate semiconductor;

a source/drain formed in the substrate adjacent the gate electrode and having an activated doped region with a first silicide layer disposed therein and wherein the activated doped region and the first silicide layer are aligned with a spacer disposed along sidewalls of the gate electrode; and

the source/drain also having an extension of the activated doped region wherein the extension has less dopant concentration than the activated doped region and the extension and a second silicide layer disposed in the extension are aligned with the gate electrode to have the less dopant concentration of the extension reside between the channel region and the activated doped region.

78. (New) The microelectronic structure of claim 77, wherein the activated doped region is thicker than the extension.

79. (New) The microelectronic structure of claim 77, wherein the first silicide layer is thicker than the first silicide layer.

80. (New) The microelectronic structure of claim 77, wherein the activated doped region and the extension comprise ion implanted material.

81. (New) The microelectronic structure of claim 77, wherein the first and second silicide layers comprise different metals.

82. (New) The microelectronic structure of claim 77, wherein the first and second silicide layers comprise a same metal.

83. (New) The microelectronic structure of claim 77, wherein the second silicide layer comprises $CoSi_2$.

84. (New) The microelectronic structure of claim 77, wherein the second silicide layer comprises $TiSi_2$.

Sub F4

85. (New) The microelectronic structure of claim 77, wherein the first silicide layer comprises nickel silicide.

86. (New) The microelectronic structure of claim 77, wherein the first silicide layer comprises $CoSi_2$.

E1

87. (New) The microelectronic structure of claim 77, wherein the first silicide layer comprises $TiSi_2$.

Concl'd Sub F5

88. (New) The microelectronic structure of claim 77, further comprising a barrier layer adjacent the gate electrode.

89. (New) The microelectronic structure of claim 88, wherein the barrier layer comprises silicon nitride.

90. (New) The microelectronic structure of claim 77, wherein the extension is approximately 300-500 angstroms in thickness.